Amendment in the Claims

1. (Currently Amended) A processor, comprising:

a Boolean logic unit, wherein the Boolean logic unit is operable for dynamically performing the short-circuit evaluation of Conjunctive Normal Form Boolean expressions/operations;

a plurality of input/output interfaces, wherein the plurality of input/output interfaces are operable for receiving a plurality of compiled Boolean expressions/operations and transmitting a plurality of compiled results; and

a plurality of registers.

2. (Original) The processor of claim 1, further comprising a plurality of AND gates, wherein the plurality of AND gates are operable for passing a plurality of expression/operation results and signals.

3. (Original) The processor of claim 2, wherein the plurality of AND gates comprise an *n*-bit AND register, wherein the *n*-bit AND register is operable for rolling up the results of conjuncts.

4. (Original) The processor of claim 3, wherein the default value of the *n*-bit AND register is 'one'.

5. (Original) The processor of claim 3, wherein the *n*-bit AND register initializes to a value of 'one' after the start of an operational code.

6. (Original) The processor of claim 3, wherein the *n*-bit AND register remains at a value of 'one' if all of the conjuncts of a Boolean expression/operation being evaluated are true.

7. (Original) The processor of claim 3, wherein the Conjunctive Normal Form Boolean expression/operation is false if the *n*-bit AND register is set to 'zero', and the remainder of the Boolean expression/operation is short-circuited.

8. (Original) The processor of claim 1, further comprising an OR gate, wherein the OR gate is operable for passing a plurality of expression/operation results and signals.

9. (Original) The processor of claim 8, wherein OR gate comprises a *n*-bit OR register, wherein the *n*-bit OR register is operable for rolling up the results of conjuncts.

10. (Original) The processor of claim 9, wherein the *n*-bit OR register initializes to a value of 'zero' and remains in that state until a state in a predetermined conjunct evaluates to 'one'.

11. (Original) The processor of claim 10, further comprising an *n*-bit OR conjunct register, wherein the *n*-bit OR conjunct register indicates that the evaluation of a conjunct comprising an OR clause has begun,

12. (Original) The processor of claim 11, wherein the *n*-bit OR conjunct register initializes to a value of 'zero' and remains in that state until an OR expression/operation sets its value to 'one'.

13. (Original) The processor of claim 11, wherein a predetermined conjunct evaluates to true if the *n*-bit OR register is set to 'one' and the *n*-bit OR conjunct register is set to 'one', and the processor short-circuits to the start of the next conjunct.

14. (Original) The processor of claim 1, further comprising an operation decoder, wherein the operation decoder is operable for deciphering an operational code and controlling units that are dependent upon the operational code.

15. (Original) The processor of claim 14, wherein functions of the operation decoder comprise Boolean AND, Boolean OR, end of operation, no operation, unconditional jump, conditional jump, start of operation, and start of conjunct.

16. (Original) The processor of claim 1, further comprising a control encoder, wherein the control encoder accepts $n+m$ bits in parallel and outputs them across a device bus either in series or in parallel.

17. (Original) The processor of claim 1, further comprising a random-access memory, wherein the random-access memory is operable for storing the states of a plurality of devices that the processor monitors and controls.

18. (Original) The processor of claim 1, further comprising a memory, wherein the memory is operable for holding a compiled micro-program.

19. (Original) The processor of claim 18, further comprising a program counter, wherein the program counter is operable for fetching an instruction from the read-only memory.

20. (Original) The processor of claim 19, further comprising a memory device, wherein the memory device is operable for configuring the program counter for normal operation, unconditional jump operation, conditional jump operation, and Boolean short-circuit operation.

21. (Original) The processor of claim 1, wherein the plurality of registers comprise a plurality of multi-bit registers.

22. (Original) The processor of claim 21, wherein the plurality of multi-bit registers comprise an instruction register, a next operation address register, and an end of OR address register.

23. (Original) The processor of claim 22, wherein the instruction register comprises an $n+m+3$-bit wide register comprising an n-bit address, an m-bit control/state word, and a 3-bit operational code.

24. (Original) The processor of claim 22, wherein the next operation register stores an address used for Boolean short-circuiting.

25. (Original) The processor of claim 22, wherein the end of OR address register stores the address of an instruction immediately following a conjunct comprising an OR clause.

26. (Original) The processor of claim 1, wherein the plurality of registers comprise a plurality of single-bit registers.

27. (Original) The processor of claim 26, wherein the plurality of single-bit registers comprise an AND truth state register, an OR truth state register, and an indicator for conjuncts comprising OR clauses.

Claims 28-45 (cancelled).